ECE 164 Project

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Page 1: Outline of the Design

Page 2: Schematic and Component Values

Page 3: Schematic (Continued)

Page 4: Macro–Model Calculations

Before analyzing the transistor-level design, we simplified the circuit into a macro-model for the folded-cascode and CS stage.

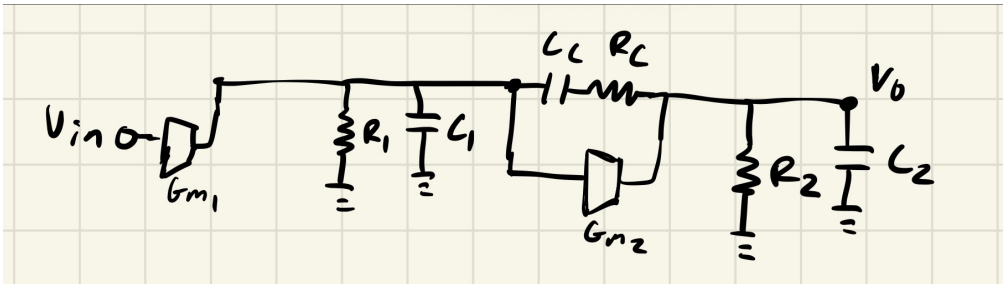

Figure 1: Macro Model.

We began by selecting a reasonable compensation capacitor $C_c \approx 1.6\,\text{pF}$ and unity-gain margin UGM $= 90\,\text{MHz}$, which allowed us to compute $g_{m1} = 2\pi \cdot \text{UGM} \cdot C_c = 955.04\,\mu\text{S}$. After reviewing class lectures and discussions, we chose an initial ratio $\frac{G_{m2}}{G_{m1}} = 5$, giving $g_{m2} = 4.775\,\text{mS}$. Because $C_2 \approx C_L$, we obtained $\omega_{p2} = \frac{G_{m2}}{C_L} = 2.116\,\text{Grad/s}$. To push the zero to infinity for the initial design, we used $\omega_z = \frac{1}{(R_C - G_{m2}^{-1})C_c} \to \infty$, which sets $R_C = 1/G_{m2} = 209.41\,\Omega$. The gain expressions $A_{v1} = G_{m1}R_1 = 52\,\text{dB}$ and $A_{v2} = G_{m2}R_2 = 23\,\text{dB}$ gave $R_1 = 417\,\text{k}\Omega$ and $R_2 = 2.96\,\text{k}\Omega$. With these values, we obtained the poles $\omega_{p1} = \frac{1}{R_2 C_2} = 106\,\text{krad/s}$ and $\omega_{p3} = \frac{1}{R_C C_c}\left(1 + \frac{C_c}{C_1}\right) = 50.7\,\text{Grad/s}$, assuming $C_1 = 100\,\text{fF}$. Finally, the phase margin was computed using $PM = 90^\circ - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right) = 75.29^\circ$.

Page 5: Common-Source Stage + Folded Cascode

We used the g_m/I_D methodology to size the devices in our design. For M9, we set $g_{m9} = G_{m1}$ and initially selected a g_m/I_D of 12.5, but later reduced it to 10 to ensure $V_{\text{ov}} \geq 150\,\text{mV}$. This gave

$$I_{D9} = I_{D8} = \frac{g_{m9}}{10}.$$

For M8, we chose a lower g_m/I_D of 6 so that it behaves as a stronger current source. Using the provided MATLAB script, we calculated the required device widths based on our chosen channel length, ensuring that the resulting output resistance $R1 = r_{o9}||r_{o8}$ was approximately equal to R_1.

For our folded cascode stage, we based our calculations on the small-signal gain

$$A_{v1} = G_{m1} r_o \approx 52,$$

the transconductance relation

$$g_{m3} = G_{m1},$$

and the output resistance expression

$$R_o = g_{m5} r_{o5} r_{o4} \Big\| g_{m6} r_{o6} \left(r_{o7b} \parallel r_{o3b} \right).$$

We selected a g_m/I_D of 10 for M3 since it satisfies the required overdrive voltage, allowing us to determine its drain current. For M1, M2, M4a, and M4b, g_m/I_D of 6,

$$\frac{g_m}{I_{D\,\{1,2,4a,4b\}}} = \frac{g_m}{I_{D\,8}} = 6,$$

since these devices serve a similar role to M8 in setting bias currents and output resistance. As a starting condition, we set the current in M4a,b to be $1.5D3$ giving us

$$I_{D7} = I_{D4} + I_{D3} = 2.5\, I_{D3},$$

We decided to be consistent with PMOS lengths which simplified biasing. Using MATLAB, we obtained the required $g_m r_o$ values and extracted device widths. For M7, we selected $g_m/I_D = 7$ as an initial point, and from the R_o expression we determined the necessary $g_m r_o$ for M6. MATLAB was then used to size M6 accordingly and complete the widths for the remaining transistors.

Page 6: Magic Battery and Constant g_m Bias Network

For both magic battery networks, we sized the devices based on the folded-cascode transistor ratios. In the PMOS magic battery, we used the width-to-length relations

$$\frac{W}{L}_{b9} = \frac{W}{L}_{b5a} = \frac{W}{L}_{b12} = \frac{W}{L}_{b13} = \frac{W}{L}_{4},$$

$$\frac{W}{L}_{b10} = \frac{W}{L}_{b6} = \frac{W}{L}_{5},$$

$$\frac{W}{L}_{b5b} = \frac{2}{3}\frac{W}{L}_{4},$$

and found that choosing $k = 3$ for M_{b5b} provided the correct gate voltages to our folded casecode. For the NMOS magic battery, we sized the devices relative to M6 and M7 using

$$\frac{W}{L}_{b14a} = \frac{W}{L}_{7},$$

$$\frac{W}{L}_{b14b} = \frac{2}{5}\frac{W}{L}_{7},$$

$$\frac{W}{L}_{b15} = \frac{W}{L}_{6},$$

and selected $k = 5$ to ensure that both M6 and M7 remain in saturation across the expected operating range.

For the constant–g_m bias circuit, we selected the bias transconductance to match g_{m3}, and used

$$G_{m1} = \frac{2\left(1 - \frac{1}{\sqrt{m}}\right)}{R_{\text{bias}}}, \qquad m = 4,$$

to compute the required resistor value

$$R_{\text{bias}} = \frac{1}{G_{m1}} \approx 1.05\,\text{k}\Omega.$$

We also matched the g_m/I_D of the bias transistors to that of M3, giving

$$\frac{g_m}{I_D}_{b1,b2,b3,b4} = 10,$$

which set the resulting bias current to

$$I_D \approx 91\,\mu\text{A}.$$

Using the provided MATLAB scripts, we determined the device dimensions that achieve these operating points and ensure proper biasing throughout the circuit.

Page 7: Power Calculations and Design Improvements

Page 8: Bode Plot Simulation Results

Page 9: Transient Simulation for 10 μVp-p at 20 Hz

Page 10: ICMR and OCMR Plots

Page 11: Comments and Conclusions